REMARKS

Summary of Office Action

The Specification is objected to for containing a typographical error in a cross reference to another application.

The Title is objected to as not being descriptive with respect to the pending claims.

Claims 1-6 are pending.

Claims 1-2 stand rejected under 35 U.S.C. §102(e), as being anticipated by *Kennedy, et al.* (U.S. Patent 6,268,457).

Claims 1-3 stand rejected under 35 U.S.C. §102(e), as being anticipated by *Chung, et al.* (U.S. Patent 6,184,142).

Claim 6 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Chung et al.* in view of *Li, et al.* (U.S. Patent 6,423,628).

Claims 4 and 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over *Chung et al.* in view of applicants' admitted prior art.

Summary of Applicant's Response

Applicants have amended the specification to correct the errors therein and to provide a more descriptive title. Applicants have also amended claims 1, 3, and 6, and added new claims 13-17 to more particularly point out and distinctly claims the subject matter they regard as the invention.

Detailed Response

The present invention relates to systems and methods for efficiently fabricating a semiconductor device of the type having different structures in different areas of the semiconductor. In a semiconductor having both logic circuitry and embedded memory, for instance, the processing requirements of the logic circuit and memory circuits differ and sometimes conflict with each other. As described in the specification, when a resist or mask layer is removed after etching structures in the embedded memory, the antireflective coating (ARC) layer is often damaged in the areas in which the logic circuitry is to be formed. This damage to the ARC layer reduced the effectiveness of the ARC layer, adversely impacting the critical dimension of the structures in the logic circuitry.

Applicants discovered that by using appropriate materials and process steps, damage to the ARC layer can be minimized when removing the resist layer. Specifically, applicants discovered that SiON may be used as an ARC layer that is resistant to a plasma etch used to remove a resist or mask. Applicants respectfully submit that this is not taught or disclosed in the prior art.

Response to Rejections
under 35 U.S.C. §102(e)

At paragraph 4 of the Office action, claims 1-2 are rejected as being anticipated by *Kennedy*. Applicants respectfully traverse this ground of rejection because Kennedy fails to disclose each and every limitation of the instant claims in that *Kennedy* fails to disclose an ARC layer comprising a layer of SiON as required by the claims. For example, amended claim 1 recites a step of:

"providing an antireflective coating (ARC) layer having antireflective properties, wherein the ARC layer comprises a layer of SiON having a thickness of less than about 500 Angstroms (Å); . . ."

At paragraph 5 of the Office action, claims 1-3 are rejected as being anticipated by *Chung*. Applicants respectfully traverse this ground of rejection because *Chung* fails to disclose all of the limitations of the present claims. Although *Chung* discloses the use of an SiON layer in semiconductor fabrication, *Chung* uses the layer as a stop layer to protect a layer of low-k dielectric from damage during etching. Moreover, *Chung* discloses that the SiON layer has a thickness of between 500 and 1000 Angstroms. Therefore, *Chung* fails to disclose an ARC layer comprising a layer of SiON of less than about 500 Angstroms in thickness as required by the present claims.

Moreover, neither *Kennedy* nor *Chung* disclose patterning a resist layer so that a first area of the semiconductor may be etched, then removing a resist layer and applying a second resist layer so that a second area of the semiconductor device may be processed, as required by the present claims. For instance, new claim 13 includes the limitations of:

"removing the first resist layer utilizing a plasma etch;

and

"depositing a second resist layer on the SiON layer; . . . "

Kennedy and *Chung* both fail to disclose these limitations and, therefore, fail to read on the claims of the present application. Accordingly, applicants respectfully submit that the present claims can be distinguished from the art of record and are allowable over such art.

Response to Rejections
Under 35 U.S.C. §103(a)

Claim 4-6 stand rejected as being obvious over *Chung* in further view of *Li* and Applicants admitted prior art. Applicants respectfully traverse this ground of rejection because none of the cited references, taken singly or in combination, disclose, teach, or otherwise suggest the claimed invention. Specifically, the references fail to teach providing an SiON ARC layer, patterning a resist layer and etching a first area of a semiconductor device, then removing the resist layer and applying a second resist layer so that another area of a semiconductor device may be processed.

Conclusion

In light of the arguments presented hereinabove, Applicants respectfully submit that the instant claims distinguish over the cited references, taken either singly or in combination. Accordingly, Applicants respectfully submit that the instant application is now in condition for allowance and should be passed to issue.

With the addition of no new claims beyond those already paid for, no additional filing fees are due. However, the Applicants request a Three Month Extension of Time to File Response (SB/22) as attached along with fees in the amount of $930.00 and the SB/17 Fee Transmittal Sheet. Also the Patent and Trademark Office is hereby authorized to charge any additional fees, or to credit any overpayment of same, to Deposit Account Number 23-2426 of WINSTEAD SECHREST & MINICK P.C.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (512) 370-2895.

Respectfully submitted,
WINSTEAD SECHREST & MINICK
Attorneys for Applicant

By: Michael Adams
Michael P. Adams
Reg. No. 34,763

P.O. Box 50784
1201 Main Street
Dallas, Texas 75250-0784
(512) 370-2895
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